AMENDMENTS TO THE SPECIFICATION

Please replace the title with the following new title:

A METHOD AND APPARATUS FOR MULTIPROCESSOR EMBEDDED DEBUGGING SUPPORT

On page 1, please replace the heading under the title as follows:

BACKGROUND

On page 1, before paragraph [002], please replace the heading as follows:

DESCRIPTION OF THE RELATED ART

On page 1, please replace the heading before paragraph [003] as follows (note the headings should not be bold or underlined):

BRIEF DESCRIPTION OF THE DRAWINGS

On page 2, please replace the heading before paragraph [0016] as follows:

DETAILED DESCRIPTION

Please amend paragraph [0024] as follows:

FIG. 4 illustrates an embodiment including an apparatus having processing chip 400 coupled to controller 430 and to memory 410, such as a RAM, static RAM (SRAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), read-only memory (ROM), etc. In one embodiment debug process 420 is initiated by controller 430. In one embodiment debug process 420 attaches at least one breakpoint bit field to each instruction of a set of instructions within a PE, such as PE 210. In one embodiment debug process attaches at least three register bit fields (run/stop, single-step, and debug enable fields) to at least one control status register within an ISP, such as ISP 110. Memory 410 can store instructions loaded into a PE 210. Processing chip 400 is coupled to memory 410 and controller 430 by a bus, such as an internal bus, a network (such as a local area network (LAN) or wide area network (WAN)), etc.

Please amend paragraph [0032] as follows:

FIG. 7A illustrates a system adaptable to use debug process 420 to perform debug functions in an instruction pipeline. In FIG. 7A the dashed line indicates system 700. System 700 can be coupled with one or more host processors ~~710~~(not shown), host interface 720, debug instruction register 730, and a plurality of general purpose registers 791. System 700 includes instruction memory 740, instruction register 750, decoder 760, execution unit 770, debug executive unit 780 coupled to debug instruction register 730 and decoder 760, ~~debug executive unit~~first mux element 781 coupled to instruction memory 740, second mux element 782 coupled to execution unit 770, and a plurality of local registers 790. The host processor includes debug process 420 for communicating and debugging system 700. In one embodiment debug process 700 attaches at least one bit field to each instruction transmitted to system 700, and attaches at least three register bit fields to a control status register. System 700 is repeated for each PE within an ISP.

Please amend paragraph [0033] as follows:

Debug process 420 running in a host processor ~~710~~ enables a user to set breakpoints, enable debugging, single step through cycles, run/stop, view the architectural states, and change or overwrite architectural states through a graphical user interface (GUI) displayed on a monitor and entered through a user interface (UI) (e.g., a keyboard, pointing device, etc.).

Please amend paragraph [0039] as follows:

Block 860 determines whether the run/stop field is enabled. If it is determined that the run/stop field is enabled, process 800 continues with block 865 where processing for the instruction pipeline runs continuously. If it is determined that the run/stop field is not set, the instruction pipeline is stopped at block 870. In one embodiment a user selects a specific ISP to run and the run bit is set in the control status register for that particular ISP.

Please amend paragraph [0047] as follows:

The above debug process embodiments can also be stored on a device or machine-readable medium and be read by a machine to perform instructions. The machine-readable medium includes any mechanism that provides (i.e., stores and/or transmits) information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read-only memory (ROM); random-access memory (RAM); magnetic disk storage media; optical storage media; and flash memory devices~~;~~. ~~biological electrical, mechanical systems; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.).~~ The device or machine-readable medium may include a micro-electromechanical system (MEMS), nanotechnology devices, organic, holographic, solid-state memory device and/or a rotating magnetic or optical disk. The device or machine-readable medium may be distributed when partitions of instructions have been separated into different machines, such as across an interconnection of computers.

On page 12, please replace the heading as follows:

CLAIMS

Please replace the abstract with the following new abstract, which is also submitted on a separate page:

ABSTRACT OF THE DISCLOSURE

A device having at least one processor is connected to a controller and a memory. The controller executes a debug process. The debug process adds a breakpoint bit field to each instruction. Also, a system includes image signal processors (ISPs). Each ISP includes processor elements (PEs). The ISPs also include a debug instruction register connected to a first mux element. An instruction memory is connected to an instruction register. A decoder is also connected to the instruction register. An execution unit is connected to the decoder. A debug executive unit is connected to the instruction memory, and a second mux element is connected to the execution unit and local registers. The decoder decodes a breakpoint bit field of each instruction.